-150V P-Channel Enhancement Mode MOSFET

Features

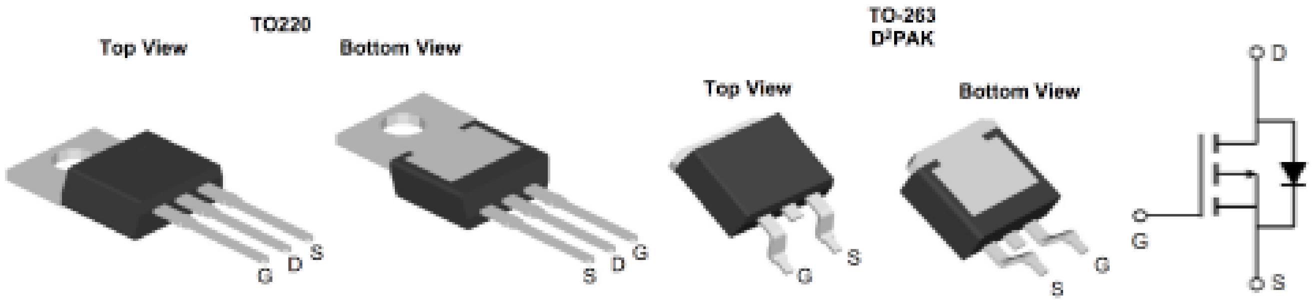
- Advanced HEFET™ Technology
- Ultra Low On-Resistance
- Excellent $Q_g x R_{DS(on)}$ Product
- 100% avalanche tested
- 175°C Operating Temperature
- Lead Free and Green Devices Available (RoHS Comp

Applications

- Motor Drives
- Uninterruptible Power Supplies
- DC/DC converter
- General Purpose Applications

V_{DS} = -150V I_D =-45A $R_{DS(ON)}$

<86mΩ @ V_{GS}=10V



Product ID	Pack	Marking	Qty(PCS)
XPX45P15TU	TO-263-3L	XPX45P15TUXXX YYYY	800
XmXQRm1RTr	TO-220-3L	XPX45P15TUXXX YYYY	1000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	-150	V
VGS	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Continuous Drain Current, -V_{GS} @ -10V[1]	-45	A
I_D@T_A=70℃	Continuous Drain Current, -V_{GS} @ -10V[1]	-27.2	A
IDM	Pulsed Drain Current[2]	-120	A
EAS	Single Pulse Avalanche Energy[3]	402	mJ
IAS	Avalanche Current	48	A
P_D@T_A=25℃	Total Power Dissipation[4]	65.8	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	62.5	˚C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	1.5	˚C/W

Electrical Characteristics (TJ =25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BVDSS	Drain to Source Breakdown Voltage	I_D=−250 A, V_{GS}=0V	−150	−175	−	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=−120 V, V_{GS}=0V	−	−	−1	nA
IGSS	Gate to Source Leakage Current	V_{GS}=±25 V, V_{DS}=0V	−	−	±100	nA
VGS(th)	Gate to Source Threshold Voltage	V_{GS}=V_{DS}, I_D=−250A	−1.2	-2.0	-3.0	V
RDS(on)	Static Drain to Source On Resistance	V_{GS}=−10V, I_D=−3 A	−	86	107	mΩ
RDS(on)	Static Drain to Source On Resistance	V_{GS}=−4.5V, I_D=−2.7 A	−	90	137	mΩ
GFS	Forward Transconductance	V_{DS}=−10V, I_D=−3 A	−	12	−	S
Ciss	Input Capacitance	V_{DS}=−75V, V_{GS}=0V, f=1MHz	−	1535	2045	pF
Coss	Output Capacitance		−	125	170	pF
Crss	Reverse Transfer Capacitance		−	6	10	pF
Rg	Gate Resistance		0.1	1.4	3	Ω
td(on)	Turn−On Delay Time	V_{DD}=−75V, I_D=−3A, V_{GS}=−10V, R_{GEN}= 6	−	12	23	ns
tr	Rise Time		−	3.3	10	ns
td(off)	Turn−Off Delay Time		−	22	36	ns
tf	Fall Time		−	9.6	20	ns
VSD	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = −3 A (Note 2)	−	−0.80	−1.3	V
trr	Reverse Recovery Time	I_F = −3 A, di/dt = 100 A/s	−	77	123	ns

Note :
1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3、The EAS data shows Max. rating . The test condition is VDD =-120V,VGS =-10V,L=0.1mH,IAS =-48A
4、The power dissipation is limited by 150℃ junction temperature
5、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

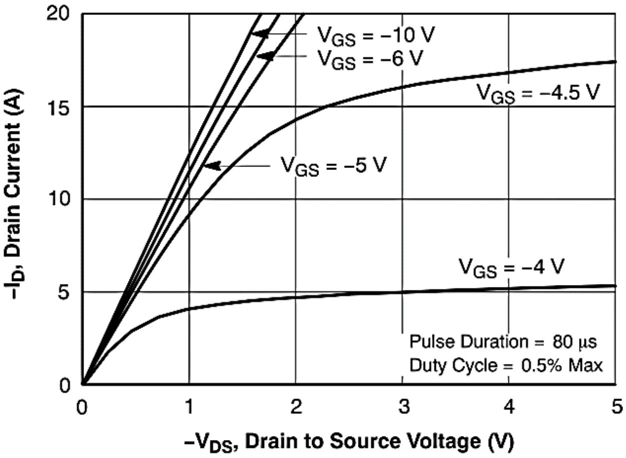


Figure 1. On Region Characteristics

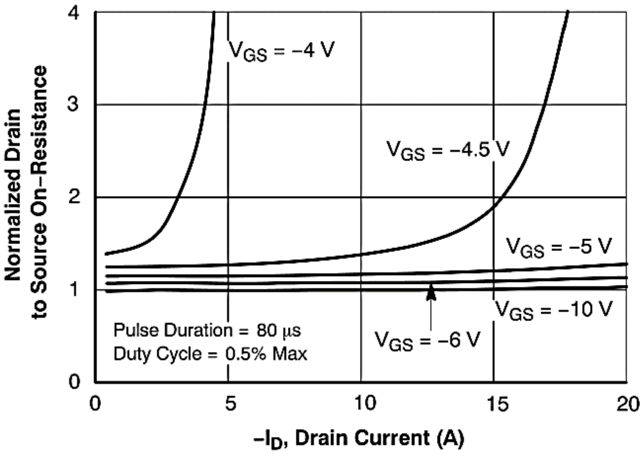


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

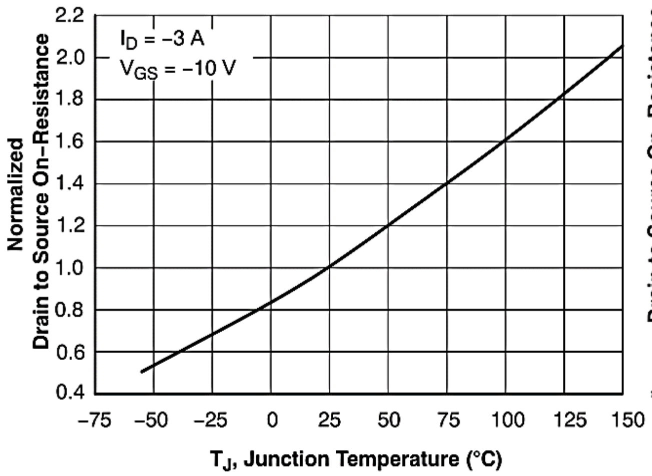


Figure 3. Normalized On Resistance vs. Junction Temperature

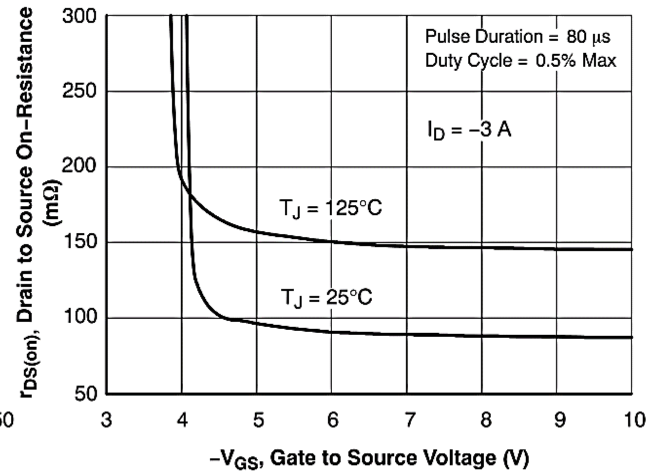


Figure 4. On−Resistance vs. Gate to Source Voltage

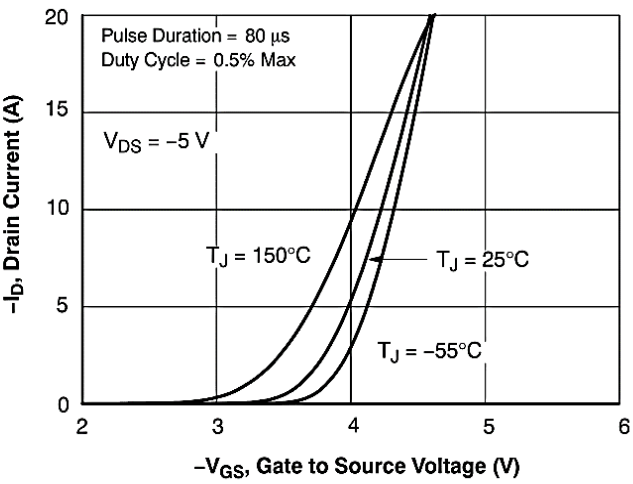


Figure 5. Transfer Characteristics

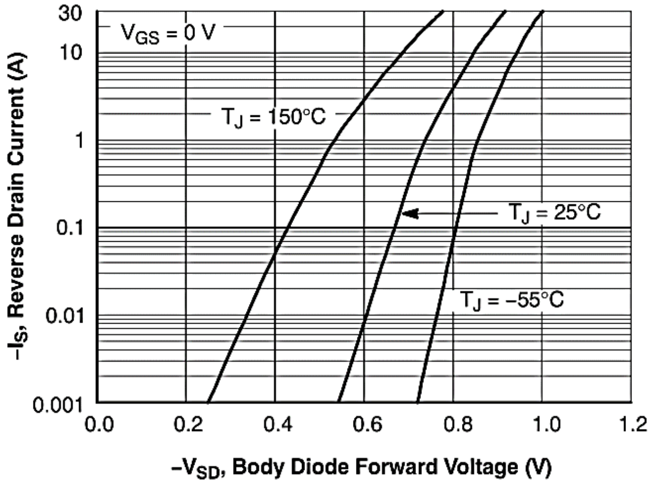


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

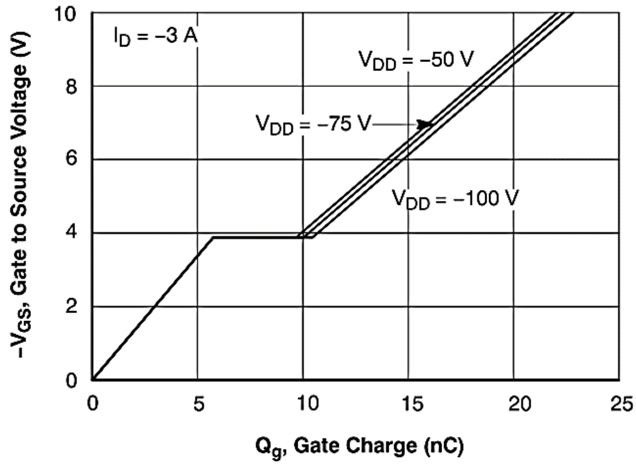


Figure 7. Gate Charge Characteristics

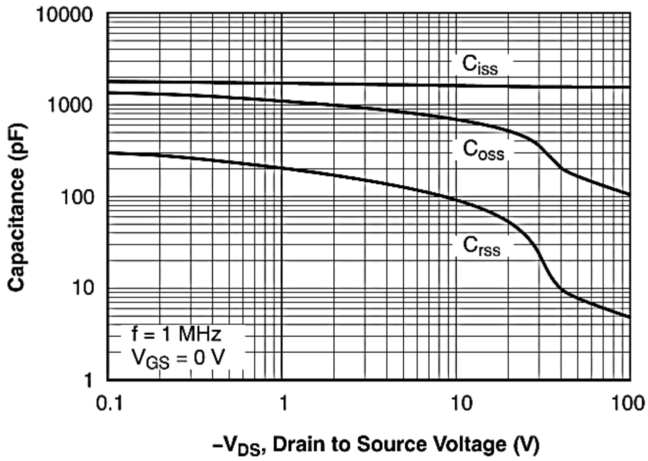


Figure 8. Capacitance vs. Drain to Source Voltage

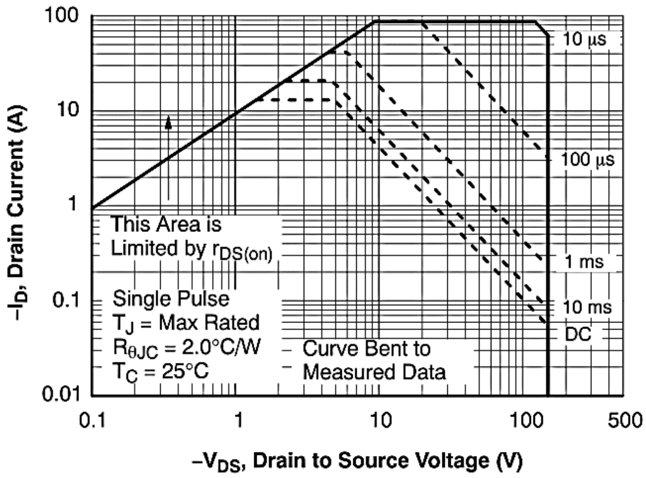


Figure 9. Forward Bias Safe Operating Area

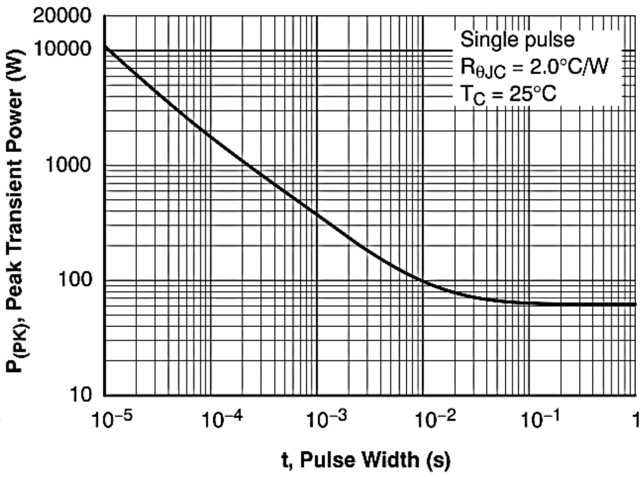


Figure 10. Single Pulse Maximum Power Dissipation

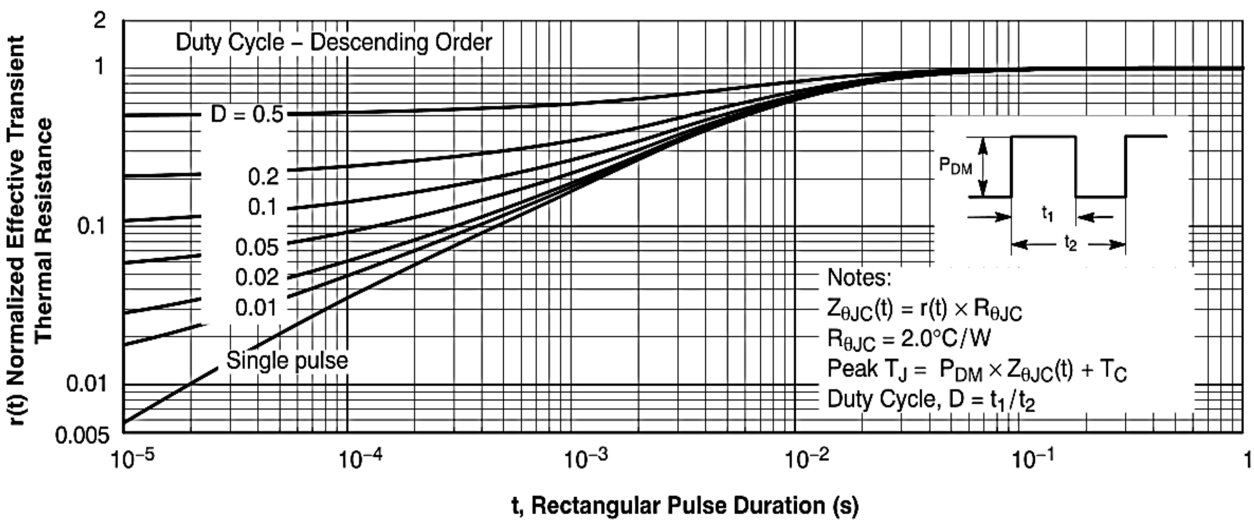
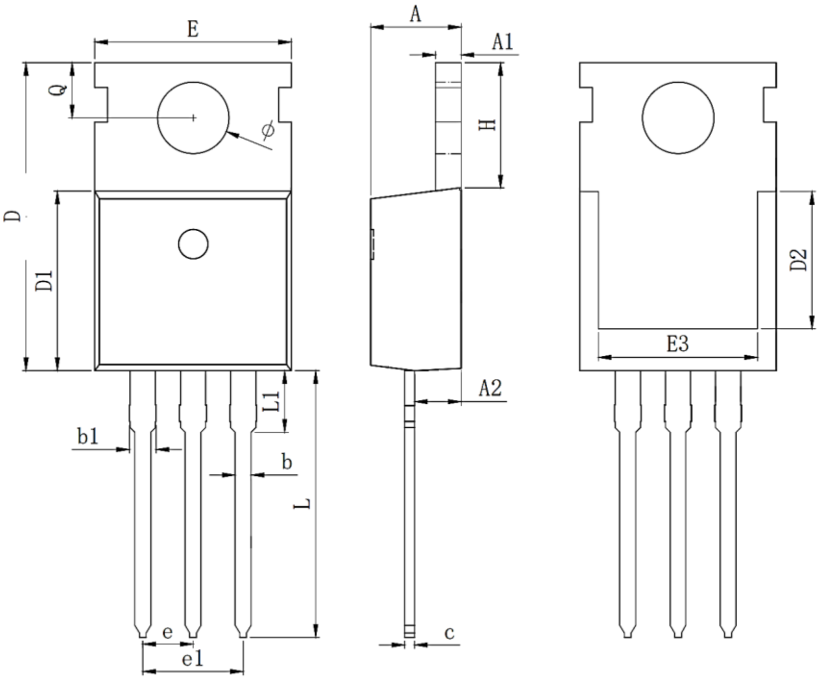


Figure 11. Junction−to−Case Transient Thermal Response Curve

Package Mechanical Data-TO-220C-3L



Symbol	Dim in mm		
	min	tpy	max
A	4.25	4.5	4.7
A1	1.15	1.3	1.45
A2	2.15	2.35	2.55
b	0.65	0.8	0.95
b1	1.15	1.35	1.55
c	0.35	0.5	0.65
D	14.3	15.3	16.3
D1	8.8	9.1	9.4
D2	6.3REF		
E	9.7	10	10.3
E3	7	8	9
e	2.54BSC		
e1	5.08BSC		
L	12.7	13.5	13.9
L1		3.1	3.4
H	6	6.5	6.85
Q	2.6	2.8	3
ϕ	3.4	3.6	3.8

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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