

Description

The XPX4012FX uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

Features

- N Channel**

40V/20A,

$R_{DS(ON)} = 16m\Omega$ (typ.) @ $V_{GS} = 10V$

$R_{DS(ON)} = 25m\Omega$ (typ.) @ $V_{GS} = 4.5V$

- P Channel**

-40V/-20A,

$R_{DS(ON)} = 30m\Omega$ (typ.) @ $V_{GS} = -10V$

$R_{DS(ON)} = 62m\Omega$ (typ.) @ $V_{GS} = -4.5V$

- 100% UIS Tested

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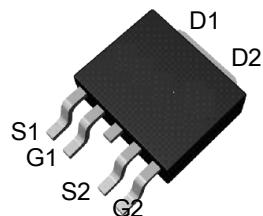
- Reliable and Rugged

Lead Free Available (RoHS Compliant)

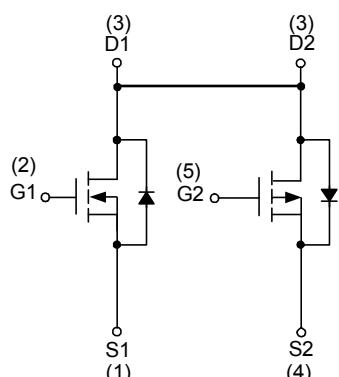
Applications

- For Fan Pre-driver H-Bridge.
- Motor Control.
- Synchronous Rectification.

Pin Description



Top View of TO-252-4



N-Channel MOSFET

P-Channel MOSFET

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XPX4012FX	XPX4012FX	TO-252-4	-	-	

**Absolute Maximum Ratings** ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N Channel	P Channel	Unit
Common Ratings				
V_{DSS}	Drain-Source Voltage	40	-40	V
V_{GSS}	Gate-Source Voltage	± 20	± 20	
T_J	Maximum Junction Temperature	175		$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 175		
I_S	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$	10	A
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$	20*	
		$T_C=100^\circ\text{C}$	20*	-15.3
I_{DM}^a	Pulsed Drain Current	$T_C=25^\circ\text{C}$	80*	-80*
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$	39.4	39.4
		$T_C=100^\circ\text{C}$	19.7	19.7
$R_{\theta JC}$	Thermal Resistance-Junction to Case	3.8		$^\circ\text{C}/\text{W}$
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$	12.2	A
		$T_A=70^\circ\text{C}$	10.2	
P_D	Power Dissipation	$T_A=25^\circ\text{C}$	6	6
		$T_A=70^\circ\text{C}$	4.2	4.2
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	$t \leq 10\text{s}$	25	25
		Steady State ^c	60	60
I_{AS}^b	Avalanche Current, Single pulse	$L=0.5\text{mH}$	10	-10
E_{AS}^b	Avalanche Energy, Single pulse	$L=0.5\text{mH}$	25	25
				mJ

Note * : Limited by package.

Note a : Pulse width limited by max. junction temperature.

Note b : UIS tested and pulse width limited by maximum junction temperature 175°C (initial temperature $T_j=25^\circ\text{C}$).

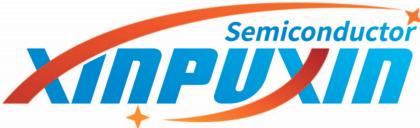
Note c : Surface Mounted on 1in^2 pad area, $t = 999\text{sec}$.

N Channel Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	N Channel			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_{\text{DS}}=250\mu\text{A}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$\text{V}_{\text{DS}}=32\text{V}, \text{V}_{\text{GS}}=0\text{V}$	-	-	1	μA
		$\text{T}_J=85^\circ\text{C}$	-	-	30	
$\text{V}_{\text{GS(th)}}$	Gate Threshold Voltage	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_{\text{DS}}=250\mu\text{A}$	1.5	2	2.5	V
I_{GSS}	Gate Leakage Current	$\text{V}_{\text{GS}}=\pm 20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	-	-	± 100	nA
$\text{R}_{\text{DS(ON)}}^{\text{d}}$	Drain-Source On-state Resistance	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_{\text{DS}}=10\text{A}$	-	16	21	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=4.5\text{V}, \text{I}_{\text{DS}}=5\text{A}$	-	18	25	
Diode Characteristics						
$\text{V}_{\text{SD}}^{\text{d}}$	Diode Forward Voltage	$\text{I}_{\text{SD}}=1\text{A}, \text{V}_{\text{GS}}=0\text{V}$	-	0.75	1.1	V
t_{rr}	Reverse Recovery Time	$\text{I}_{\text{DS}}=10\text{A}, \frac{d\text{I}_{\text{SD}}}{dt}=100\text{A}/\mu\text{s}$	-	13	-	ns
Q_{rr}	Reverse Recovery Charge		-	8.7	-	nC
Dynamic Characteristics ^e						
R_{G}	Gate Resistance	$\text{V}_{\text{GS}}=0\text{V}, \text{V}_{\text{DS}}=0\text{V}, \text{F}=1\text{MHz}$	-	2.5	-	Ω
C_{iss}	Input Capacitance	$\text{V}_{\text{GS}}=0\text{V}, \text{V}_{\text{DS}}=20\text{V}, \text{Frequency}=1.0\text{MHz}$	-	815	-	pF
C_{oss}	Output Capacitance		-	95	-	
C_{rss}	Reverse Transfer Capacitance		-	60	-	
$\text{t}_{\text{d(ON)}}$	Turn-on Delay Time	$\text{V}_{\text{DD}}=20\text{V}, \text{R}_{\text{L}}=20\Omega, \text{I}_{\text{DS}}=1\text{A}, \text{V}_{\text{GEN}}=10\text{V}, \text{R}_{\text{G}}=6\Omega$	-	7.8	-	ns
t_{r}	Turn-on Rise Time		-	6.9	-	
$\text{t}_{\text{d(OFF)}}$	Turn-off Delay Time		-	22.4	-	
t_{f}	Turn-off Fall Time		-	4.8	-	
Gate Charge Characteristics ^e						
Q_{g}	Total Gate Charge	$\text{V}_{\text{DS}}=20\text{V}, \text{V}_{\text{GS}}=10\text{V}, \text{I}_{\text{DS}}=10\text{A}$	-	15.7	22	nC
Q_{g}	Total Gate Charge	$\text{V}_{\text{DS}}=20\text{V}, \text{V}_{\text{GS}}=4.5\text{V}, \text{I}_{\text{DS}}=10\text{A}$	-	7.5	10.5	
Q_{gth}	Threshold Gate Charge		-	1.85	-	
Q_{gs}	Gate-Source Charge		-	3.24	-	
Q_{gd}	Gate-Drain Charge		-	2.75	-	

Note d : Pulse test ; pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

Note e : Guaranteed by design, not subject to production testing.

**P Channel Electrical Characteristics** ($T_A = 25^\circ\text{C}$ unless otherwise noted)

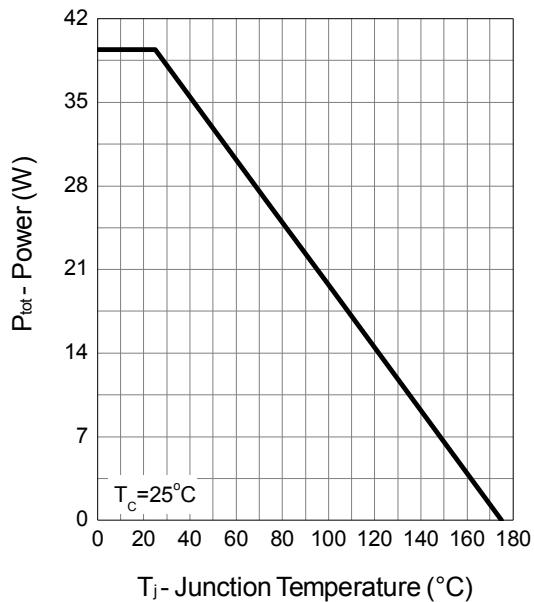
Symbol	Parameter	Test Conditions	P Channel			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{DS}}=-250\mu\text{A}$	-40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=-32\text{V}, V_{\text{GS}}=0\text{V}$ $T_J=85^\circ\text{C}$	-	-	-1	μA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{DS}}=-250\mu\text{A}$	-1.5	-2	-2.5	V
I_{GSS}	Gate Leakage Current	$V_{\text{GS}}=\pm20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	±100	nA
$R_{\text{DS(ON)}}^{\text{d}}$	Drain-Source On-state Resistance	$V_{\text{GS}}=-10\text{V}, I_{\text{DS}}=-10\text{A}$	-	30	38	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}, I_{\text{DS}}=-5\text{A}$	-	46	62	
Diode Characteristics						
V_{SD}^{d}	Diode Forward Voltage	$I_{\text{SD}}=-1\text{A}, V_{\text{GS}}=0\text{V}$	-	-0.75	-1	V
t_{rr}	Reverse Recovery Time	$I_{\text{DS}}=-10\text{A}, dI_{\text{SD}}/dt=100\text{A}/\mu\text{s}$	-	15	-	ns
Q_{rr}	Reverse Recovery Charge		-	8	-	nC
Dynamic Characteristics ^e						
R_{G}	Gate Resistance	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=0\text{V}, F=1\text{MHz}$	-	8	-	Ω
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-20\text{V}, \text{Frequency}=1.0\text{MHz}$	-	668	-	pF
C_{oss}	Output Capacitance		-	98	-	
C_{rss}	Reverse Transfer Capacitance		-	72	-	
$t_{\text{d(ON)}}$	Turn-on Delay Time	$V_{\text{DD}}=-20\text{V}, R_{\text{L}}=20\Omega, I_{\text{DS}}=-1\text{A}, V_{\text{GEN}}=-10\text{V}, R_{\text{G}}=6\Omega$	-	8.7	-	ns
t_{r}	Turn-on Rise Time		-	7	-	
$t_{\text{d(OFF)}}$	Turn-off Delay Time		-	31	-	
t_{f}	Turn-off Fall Time		-	17	-	
Gate Charge Characteristics ^e						
Q_{g}	Total Gate Charge	$V_{\text{DS}}=-20\text{V}, V_{\text{GS}}=-10\text{V}, I_{\text{DS}}=-10\text{A}$	-	15	-	nC
Q_{g}	Total Gate Charge	$V_{\text{DS}}=-20\text{V}, V_{\text{GS}}=-4.5\text{V}, I_{\text{DS}}=-10\text{A}$	-	7.5	-	
Q_{gth}	Threshold Gate Charge		-	1.4	-	
Q_{gs}	Gate-Source Charge		-	2.4	-	
Q_{gd}	Gate-Drain Charge		-	3.5	-	

Note d : Pulse test; pulse width $\leq300\mu\text{s}$, duty cycle $\leq2\%$.

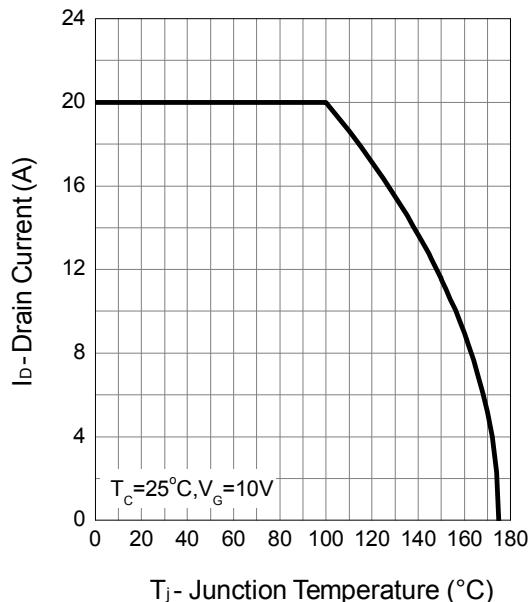
Note e : Guaranteed by design, not subject to production testing.

N Channel Typical Operating Characteristics

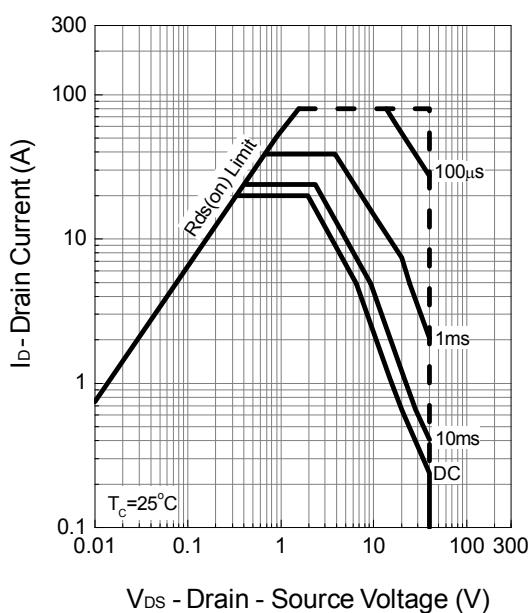
Power Dissipation



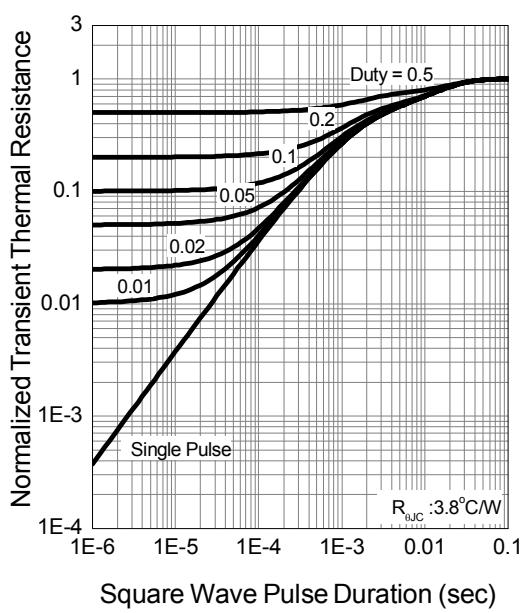
Drain Current



Safe Operation Area

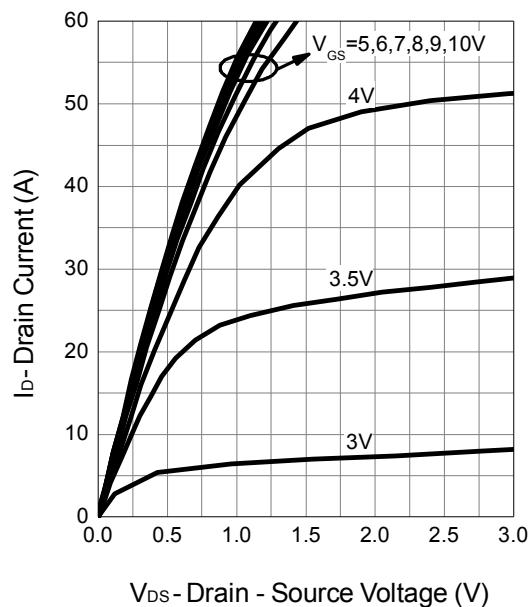


Thermal Transient Impedance

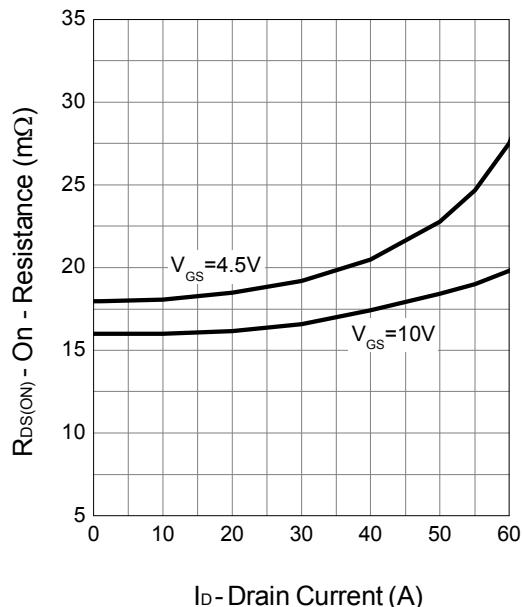


N Channel Typical Operating Characteristics (Cont.)

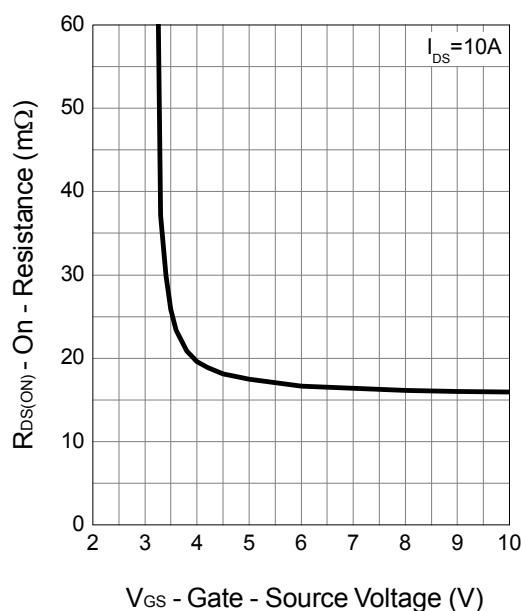
Output Characteristics



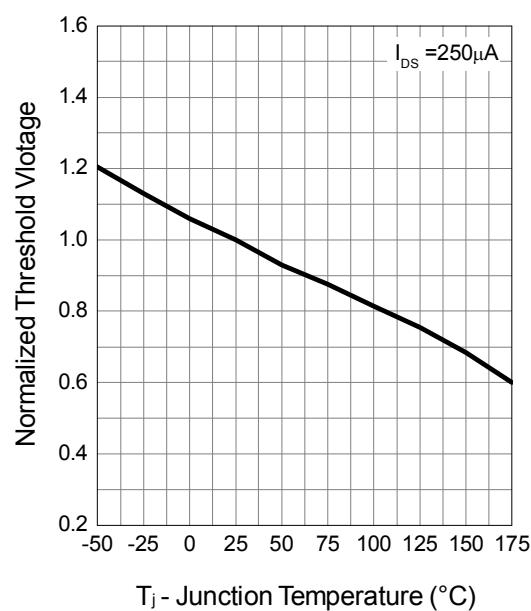
Drain-Source On Resistance



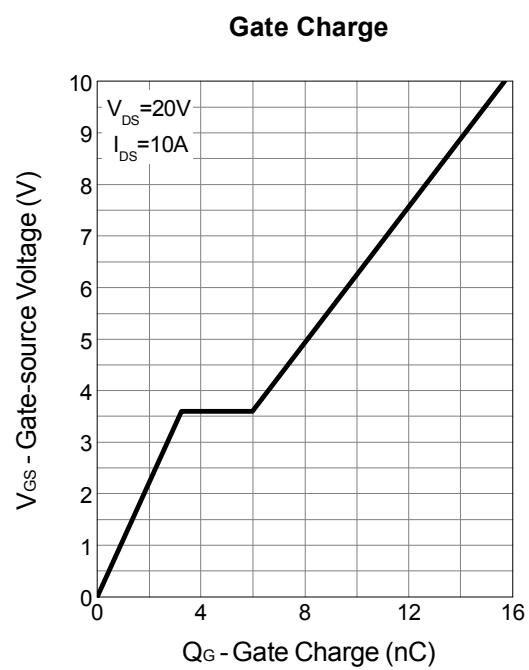
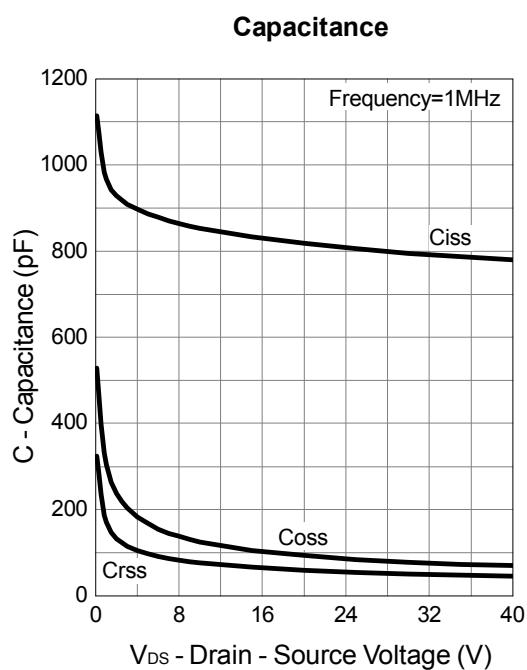
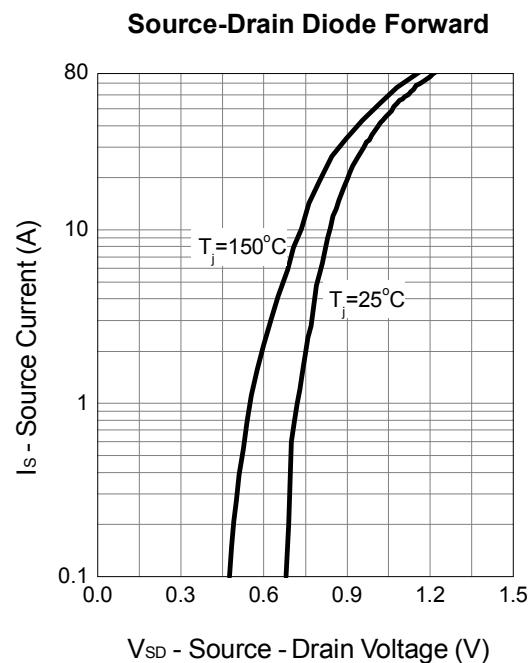
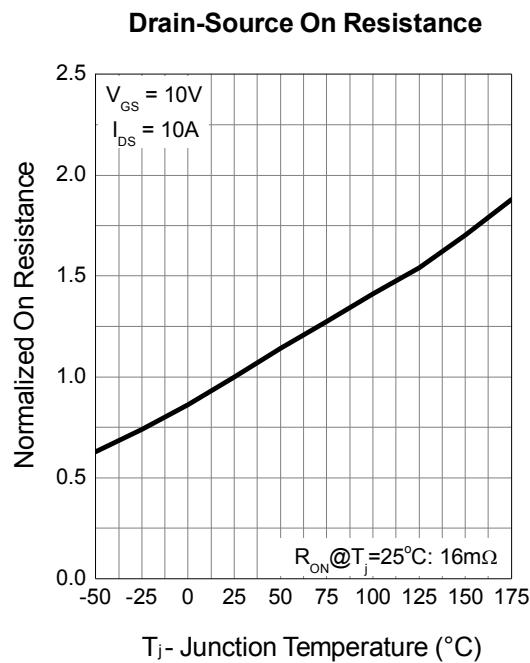
Gate-Source On Resistance



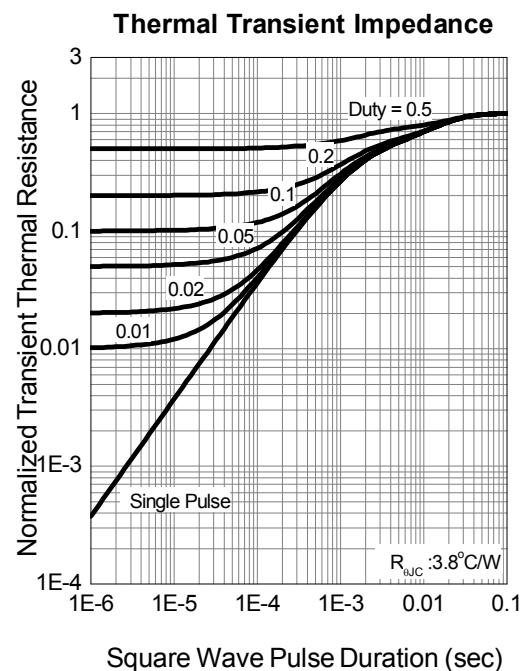
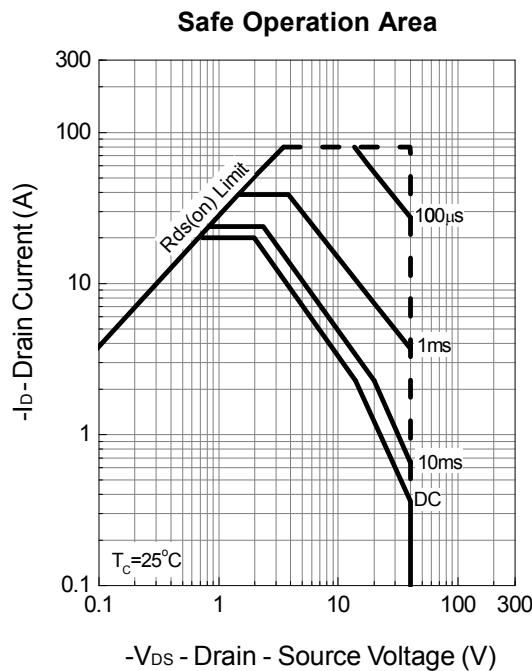
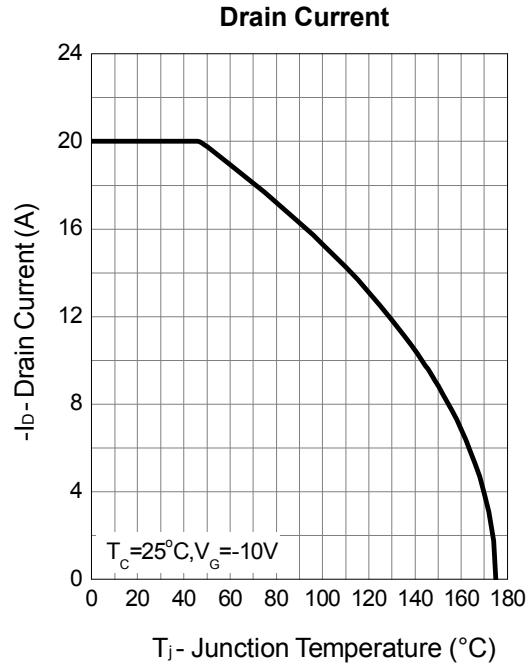
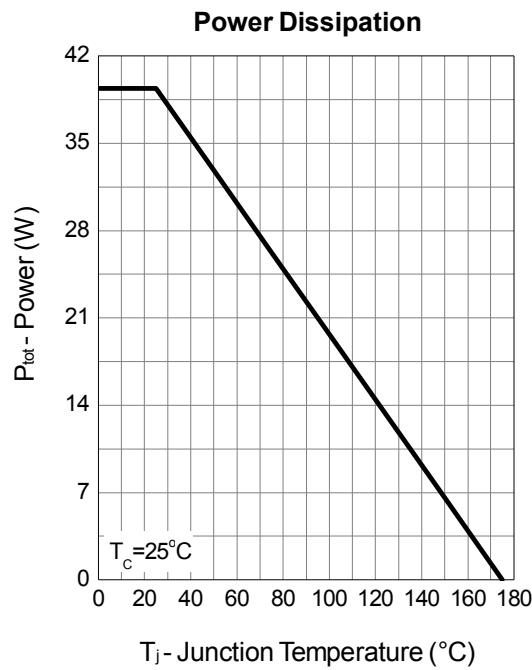
Gate Threshold Voltage



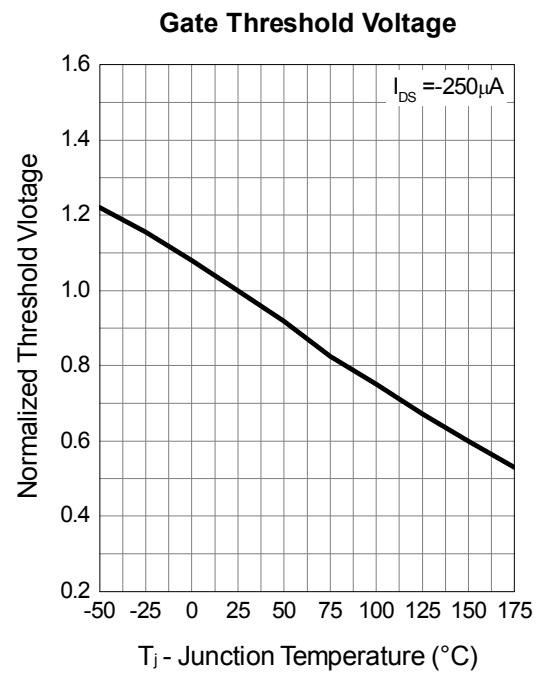
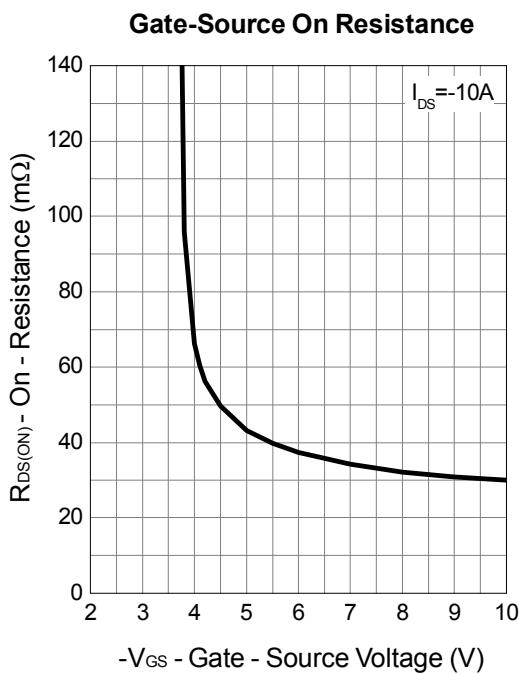
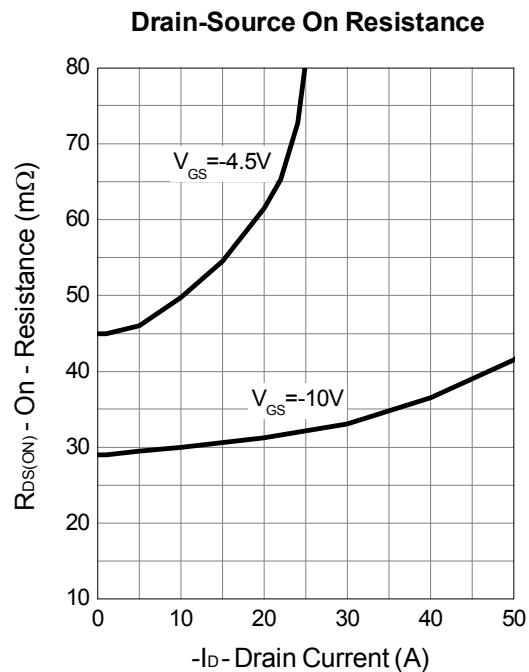
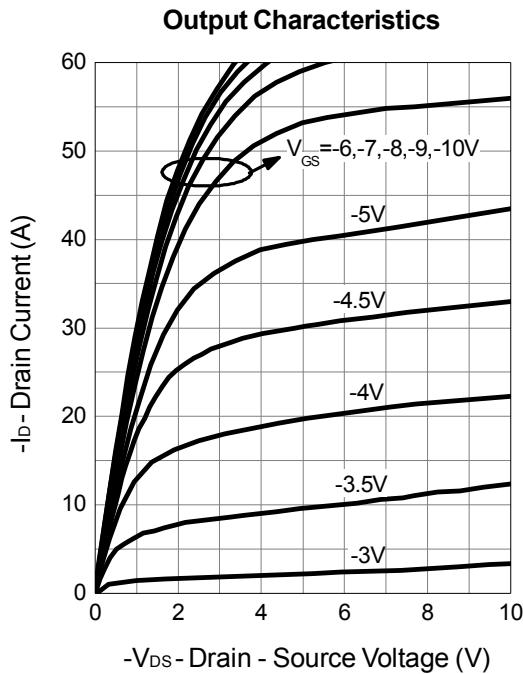
N Channel Typical Operating Characteristics (Cont.)



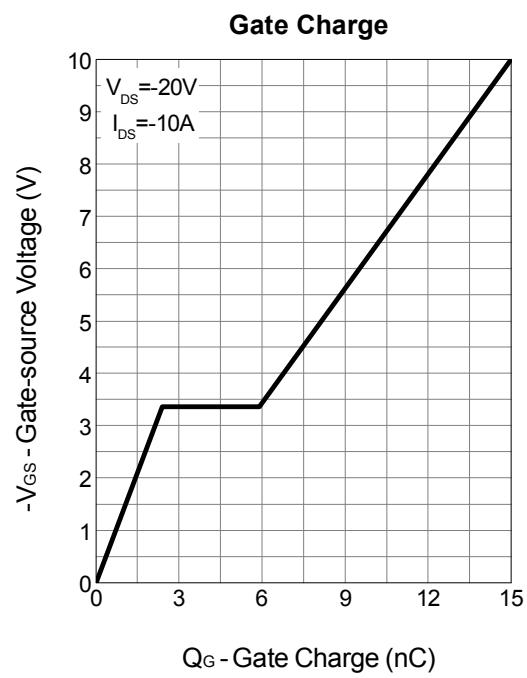
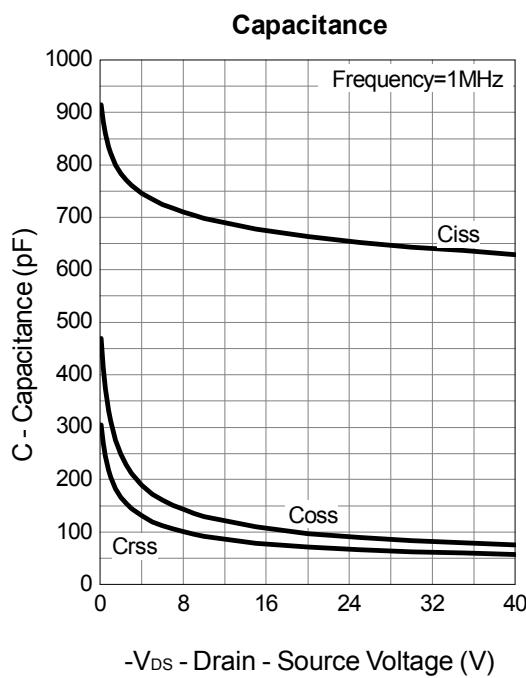
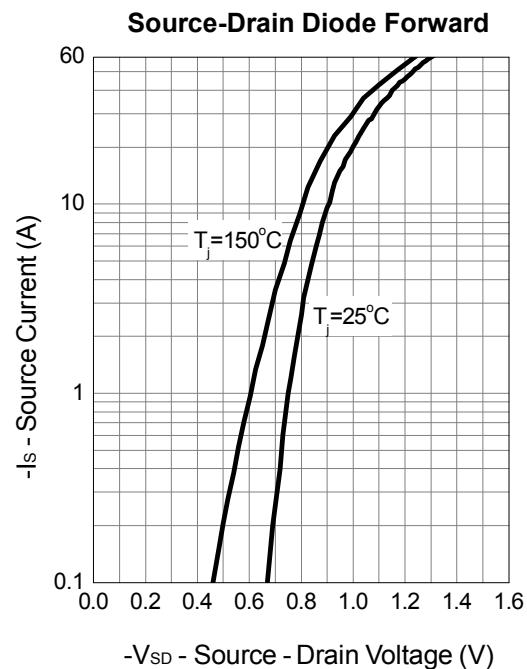
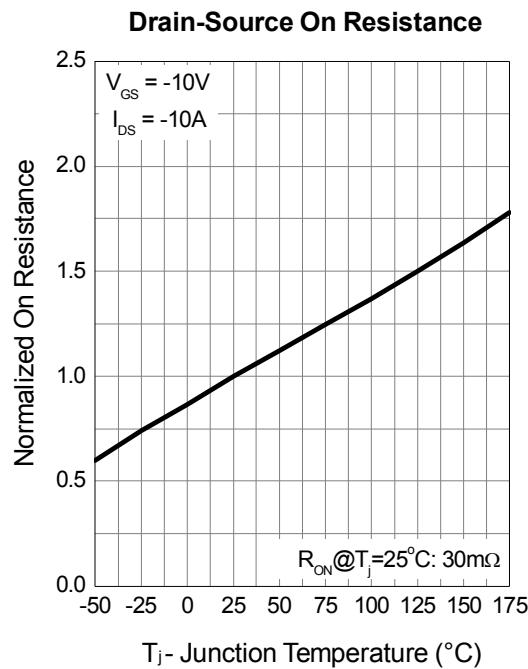
P Channel Typical Operating Characteristics



P Channel Typical Operating Characteristics (Cont.)

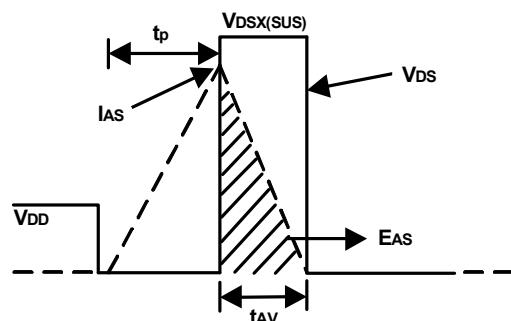
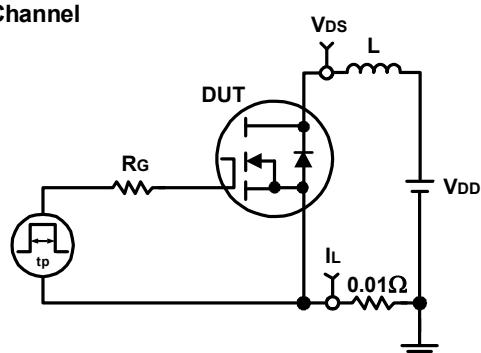


P Channel Typical Operating Characteristics (Cont.)

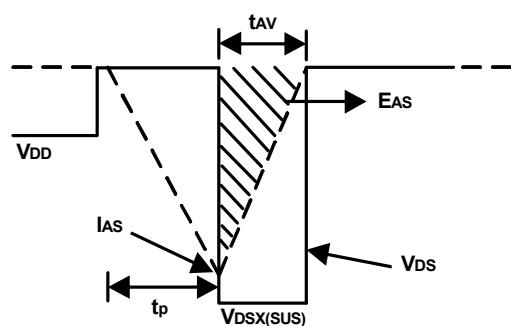
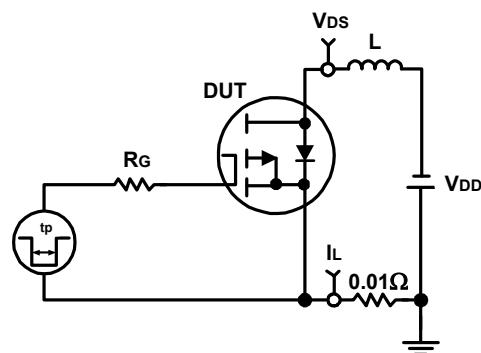


Avalanche Test Circuit and Waveforms

N Channel

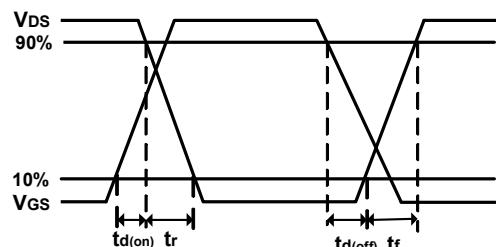
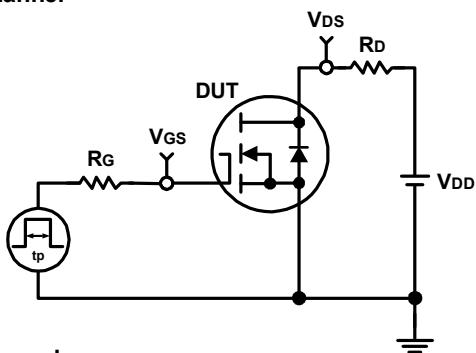


P Channel



Switching Time Test Circuit and Waveforms

N Channel



P Channel

